



# Comprehensive Functional Verification (CFV)

## Overview

Functional Verification is one of the most time-consuming processes in ASIC design cycle; yet a structured introductory course/training/education on this topic is often missing. Neither the educational institutes offer this nor there are vendors offering such training. While several language specific courses are offered by EDA vendors, a comprehensive training on fundamentals of functional verification is lacking. CFV course gives you an in-depth introduction to the different aspects of functional verification including different testbench architectures, their relative merits, demerits, areas of application of each architecture etc. CFV then delves into what is a good testbench, and elements of a modern day testbench. It covers all aspects of functional verification ranging from verification architecture to building testbenches, gate level simulation and various technologies used in verification such as simulation, formal, emulation

## Objectives

- ❖ To explore what is verification and why it is needed and how it is achieved.
- ❖ To examine the different testbench architectures available
- ❖ To explain key features of a good testbench
- ❖ To suggest widely used guidelines and need for a methodology
- ❖ To elaborate on all the different terminologies, buzz words used in the industry
- ❖ To introduce different stages in functional verification such as RTL simulation, gate level simulation, emulation etc. and to address the challenges in each one of them

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## **Duration**

One day, consisting of sessions and labs. On a need basis we can also customize it to suit our customer's need. By default we conduct public classes in Bangalore, but for a sizeable audience we can do it onsite using your preferred tool set.

## **Target audience and Prerequisites**

Primarily meant for those who are fresh into the area of functional verification including:

fresh graduates, experienced engineers having spent several years in other aspects of ASIC design such as back-end, RTL design etc.

Given the broad coverage of this course, managers who have been given the task of overseeing verification but have spent their earlier days in others aspects of ASIC design also find this course very useful. Students pursuing post graduation is VLSI and willing to explore functional verification as a potential research area will also benefit from this course as it clearly lays out standard industry practices in functional verification.

Candidates must be familiar with Verilog/VHDL; prior experience in ASIC design will be very useful though not mandatory.

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### Enrolling for a class

Send an email to [training@noveldv.com](mailto:training@noveldv.com), [cvc.training@gmail.com](mailto:cvc.training@gmail.com) with details such as:

Name:  
Company Name:  
Email ID:  
Contact Number:  
Preferred dates:

If you are coordinating for an entire team, kindly mention how many attendees are expected.

## Table of Contents

### Session 1: Introduction

- ASIC Design Flow
- Paradigm Shift
- Verification Challenge
- A quick Verification 101

### Session 2: Different Verification Technologies

- Simulation based
- Formal methods
  - Equivalence checking
  - Model checking
  - Theorem Proving
- Hybrid
- Emulation
  - FPGA based
  - Processor based

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### Session 3: Verification Metrics

- Code Coverage
- Assertion coverage (Control Centric)
- Functional Coverage (Data centric)

### Session 4: Testbench

- What is a testbench
- Basic testbenches
  - Rudimentary
  - TCL based
  - HDL based – basic ones

### Session 5: Sophisticated Testbenches

- Procedure based
- File IO based
- ASM based
- PLI based
- Layer based

### Session 6: Testbench Process

- Strategy
  - GAME
- Environment
- Testcase

### Session 7: Elements of a good testbench

- Generate (G)
  - Driver
  - Generator

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- Apply (A)
  - Scoreboard
  - Checkers

Session 8: Elements of a good testbench

- Monitor (M)
  - Passive monitor
  - Active monitor
- Examine/Evaluate(E)
  - Code coverage
  - Functional coverage
  - Assertion Coverage

Session 9: Tips and Guidelines

- Methodology
- Practical tips

Session 10: Peripheral Activities

- GLS, SDF
- Version Control
- Regression
- Role of scripts
- Verification Management

Session 11: Misc

- Unix basics
- Tool flow

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