

Verification with 'e'

What is 'e' ?

'e' is a hardware verification language (HVL) and an IEEE standard. The tool that supports e at present is Specman. 'e' can interact with Simulators using PLI. It has rich set of constructs that suits higher abstraction level of the modern day sophisticated TB's.

Overview

CVC's 'e' course gives you an in-depth introduction to the language, together with guidelines and methodologies to help you create, manage and debug effective assertions for complex design properties. The course is packed full of examples and case studies to demonstrate real life applications of the language. We also examine different approaches to coding assertions, including workarounds for the restricted language support of some tools.

Duration

1 day. We can also offer standard or customized versions of this workshop onsite or at the location of your choice.

Objectives

- To explain the advantages of hardware verification language (HVL) using 'e'.
- To describe in detail the boolean, temporal, verification layers of 'e' and show how the layers are used to build VE.
- To demonstrate, with examples, good and bad 'e' coding styles and show workarounds for simulators with language support issues.

Prerequisites

Delegates must be able to read, write and understand HDL's like VHDL / Verilog code, and be familiar with running and debugging HDL simulations. The workshop assumes no prior knowledge of e.