

# System Verilog for Design (SVD)

✦ **Intended for RTL Designers, Micro-architects**

✦ **1 day with labs**

✦ **Brief TOC**

- **Introduction**
- **Data types**
- **Interface**
- **Procedural block enhancements**
- **Enhanced Loops**
- **Arrays, Dynamic arrays, Queues – methods**
- **Compiler Directives**
- **Packages**

## Enrolling for a class

Send an email to [cvc.training@noveldv.com](mailto:cvc.training@noveldv.com) with details such as:

Name:

Company Name:

Email ID:

Contact Number:

Preferred dates:

If you are coordinating for an entire team, kindly mention how many attendees are expected.