

**CONTEMPORARY VERIFICATION CONSULTANTS
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Verification with PSL

1. What is PSL?

The Property Specification Language (PSL) is an extension to VHDL and Verilog which allows sophisticated, multi-cycle assertions and functional checks to be embedded in HDL code. PSL allows simple HDL boolean expressions to be built into complex definitions of design behavior, which can be used for assertions, functional coverage and formal verification.

2. Overview

CVC's PSL course gives you an in-depth introduction to the language, together with guidelines and methodologies to help you create, manage and debug effective assertions for complex design properties. The course is packed full of examples and case studies to demonstrate real life applications of the language. We also examine different approaches to coding assertions, including workarounds for the restricted language support of some tools.

3. Duration

2 days. We can also offer standard or customized versions of this workshop onsite or at the location of your choice.

4. Objectives

- To explain the advantages of Assertion Based Verification (ABV) using the Property Specification Language (PSL).
- To describe in detail the boolean, temporal, verification and modeling layers of PSL and show how the layers are used to build assertions.
- To demonstrate, with examples, good and bad PSL coding styles and show workarounds for simulators with language support issues.
- To describe, with case studies, a methodology for describing complex transaction-based assertions and properties using PSL. We provide an AMBA PSL property set as case study to explore full power of PSL.

5. Prerequisites

Delegates must be able to read, write and understand VHDL or Verilog code, and be familiar with running and debugging HDL simulations. The training assumes no prior knowledge of PSL.

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Property Specification Language

Table of Contents

1. Introduction to ABV & PSL Basics – Day1

Introduction

- Introduction to Assertions & ABV
- Effectiveness of Assertions and results of practical, real life projects

RTL Designer's quick start with ABV - Introduction to Checker library

- Open Verification Library (OVL)
- Mentor specific libraries
 - Questa Verification Library (QVL)
 - 0-in Checkerware
- Cadence - Incisive Assertion Library (IAL)
- Synopsys - VMM checker Library

PSL - Basics

Introduction

- Introduction to PSL
- Structure of an assertion

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PSL Layers

- Boolean Layer
- Temporal Layer
- Verification Layer
- Modeling Layer

Use Model

- In-lined
- Vunit

Sequences & SERE

- Declaration/structure
- Operations
 - Construction
 - Repetition
 - Consecutive
 - Non-consecutive
 - Go to

Foundation Language and its operators

- Declaration/Structure
- Implication
- Occurrence
- Termination

2. PSL – Advanced Day 2

Advanced PSL sequences

- Recap on basic PSL

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- Advanced PSL Sequences
 - Implication
 - Eventuality
 - Composition Operators
 - Before
 - Within
 - whilenot
- Named sequences and Endpoint
- Clocked SERE
- Parameterized sequences

Advanced PSL properties

- Advanced PSL property operators
 - terminating
- Parameterized properties
- Using functions with properties

Advanced topics

- Built-in functions
- Forall
- One shot assertions
- Recursive properties
- Assertion Overlapping
- Multiple threads
- Comments

Use models, Guidelines and common errors

- Guidelines
- Common errors
- Flow

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