

Verification Methodology Manual

What is VMM?

Verification Methodology Manual (VMM) is a framework for Verification using SystemVerilog (SV). SV is a major extension to Verilog2001, adding significant new features to Verilog for verification, design and synthesis. VMM provides a mean of doing verification in a well defined and structured way.

Overview

CVC's VMM course gives you an in-depth introduction to the main enhancements that VMM offers, discussing the benefits and issues with the new features and demonstrating how design and verification is more efficient and effective when using SystemVerilog constructs. The course breaks down into two modules. The Design module examines improvements for RTL design and synthesis; and the Verification module explores verification enhancements such as object-oriented design, assertions and randomization.

Duration

3 days Verification module. . We can also offer standard or customized versions of this workshop onsite or at the location of your choice.

Objectives

- To explore the new features of VMM verification and demonstrate the improvements in design efficiency from their use.
- To explain key features for verification, such as classes, randomization and assertions, and illustrate how to exploit these features for more efficient verification and testbench design.

Prerequisites

Delegates must be familiar with System Verilog and ideally, but not essentially, Verilog2001. If you have queries on these prerequisites, please contact CVC.